UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
08/619,203	03/21/96	KEENE	D CRUS-0045

LM51/1218
ROBERT PLATT BELL & ASSOCIATED, P. C.
917 DUKE STREET
ALEXANDRIA VA 22314

EXAMINER	
NGUYEN, F	
ART UNIT	PAPER NUMBER
2774	

DATE MAILED: 12/18/97

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

OFFICE ACTION SUMMARY

☐ Responsive to communication(s) filed on _____.

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 D.C. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire three month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☑ Claim(s) 1 through 22 is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☑ Claim(s) 1 through 22 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☑ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☑ Notice of Reference Cited, PTO-892

☑ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

-- SEE OFFICE ACTION ON THE FOLLOWING PAGES --

★ U.S. GPO: 1996-410-238/40050

DETAILED ACTION

Drawings

1. The drawing amendment submitted on 03/04/97 is acknowledged by the examiner.

Specification

2. The disclosure is objected to because of the following informalities: excessive use of verb "may" throughout the specification(e.g. page 2, lines 21, 24 and 26), typing error of word "retrieved"(page 4, line 18), "therefor"(page 8, line 13), "areas"(page 19, line 6).

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. Claims 1 through 11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 1 recites the limitation "said at least one memory configuration register" in line 9(page 24). There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keene, further in view of Dresser et al., further in view of Bril et al., and further in view of Eglit et al.

7. In reference to **claims 1 and 12,** reference Keene(U.S. Patent 5,553,220) discloses a method and apparatus for managing audio data by the use of host CPU (111), host CPU bus (109), a multimedia adapter (202) with host CPU interface (210), video graphic controller (209), video display memory RAM (101), display memory controller and arbitrator (211)(see figure 2, and column 3, lines 9-12, column 17, lines 13-14). However, it fails to expressly teach a memory configuration register, video data in component YUV format, storage of data in pixel video format. Reference Dresser et al.(U.S. Patent 5,446,8600) discloses the use of an apparatus for determining a computer memory configuration of memory modules by using a memory controller (14), a register (50), a memory configuration register (90), comparators (62), (64), (66) , (68), and data selectors (72), (74), (76), and (78)(see figure 4, column 5, lines 21-23, lines 41-43. Reference Bril et al.(5,611,041) discloses an apparatus and method for optimizing memory data bandwidth wherein video data stored in display memory (401) is in compressed format YUV 4:2:2,(e.g.data in a sixteen bit per pixel format is compressed into an eight bit per pixel equivalent format in converter/compressor (416)). It also teaches the use of an aperture control signal (452) for controlling a range of memory addresses which an external CPU or external CPU host bus writes data into display memory (401); it further discloses that, in case of PCI bus is in use with host CPU, two apertures can be utilized for writing data. This

implies that video data addresses are organized within a predetermined address range(see figure 1, column 5, lines 28-31, column 6, lines 16-23, lines 50-56). However, it does not teach the storage of video data in pixel video format. Reference Eglit et al.(U.S. Patent 5,642,139) teaches an apparatus and method wherein a PCMCI video card (500) with converters (511), (607), memory (504), is used for transmitting motion video after compressed motion video data are decompressed and converted into pixel format for display purpose on flat panel display (106), a CRT or television (see figures 3, 5, and 6, column 5, lines 1-5, column 7, lines 17-21, lines 48-50, and column 8, lines 14-20). It would have been obvious for a person of ordinary skill in the art at the time of the invention to utilize the multimedia adapter and method taught by Keene then construct a memory configuration register interfacing the display memory controller as taught by Dresser et al., then construct an aperture control scheme and apply a method for compressing video data in YUV 4:2:2 format as taught by Bril et al., then apply a method for converting decompressed video data in scan-line format as taught by Eglit et al. to obtain the combined method/apparatus (Keene, Dresser et al., Bril et al., Eglit et al.) because it would result in efficient allocation and use of memory as taught by Keene(see column 3, lines 17-18), reduction of software and hardware utilization as taught by Dresser et al.(see column 2, lines 1-3), optimal data bandwidth of memory while minimizing data buffer size and reduction of discontinuity in data flow as taught by Bril et al.(see column 4, lines 25-31), capability of transmission as well as display of color image under restricted bandwidth condition as taught by Eglit et al.(see column 3, lines 46-47). This corresponds to the claimed display controller

and method for assisting decoding of video data by receiving video data in component YUV format and storing the video data to a display memory in pixel video format.

8. In reference to **claims 2, 3, 4, 5, 6, 13 ,14, 15, 16 and 17,** reference (Keene, Dresser et al., Bril et al., Eglit et al.) further discloses a compression/serializing scheme of video data with Y0, Y1, Y2 , Y3 as luminance data and U and V as chrominance data, utilizing video memory (110), FIFO (601), multiplexer (602) and data address organizing scheme using byte lanes(U, L, bitmap sections), computing address with starting address and window MVW and offset (illustrated in divided sections for U/L, U/L for U,V, Y bitmaps , UV bitmaps). It illustrates how 480W for one 8x640 pixels block fits in one page of memory and also discloses that data are grouped per scan lines (see Eglit et al. figures 3, 4, 5, and 6, column 5, lines 6-15, column 6, lines 11-20, column 7, lines 61-63, column 9, lines 21-35). This corresponds to the claimed display controller and associated method wherein video data comprises luminance data as first contiguous data block and chrominance difference data as second contiguous data block , received and stored in byte lanes within display memory by the display memory controller , comprising one frame of luminance and chrominance difference data.

9. Claims 7, 8, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keene, further in view of Dresser et al., further in view of Bril et al., and further in view of Eglit et al. and further in view of Coelho et al.

10. In reference to claims **7, 8, 18 and 19,** reference (Keene, Dresser et al., Bril et al., Eglit et al.) fails to expressly teach how each pair of the plurality of pairs of byte lanes stores pairs of luminance data for one line of one frame of video data. Reference Coelho et al.(U.S. Patent 5,666,137) discloses that YUV9 method is well-known in the art, wherein a frame can be divided into 4x4 blocks(e.g. the screen comprising 30 bands 40 blocks wide is organized with 8 bits for U and 8 bits for V to provide color information for all 16 pixels in a block, yielding an average of one bit per pixel, thus YUV9) and the original full data Y,U, V values comprises (Y_{11}... $Y_{120\,160}$),(U_{11}... $U_{120\,160}$) and (V_{11}... $V_{120\,160}$) respectively, wherein U and V data are not all sent; a portion of row 1 illustrated with first block B11 and address P11 corresponds to the claimed line of one frame of video data (see figure 2, column 1, lines 34-52). It discloses an improved technique for formatting YUV subsampled data(see figures 3, 4, column 2, lines 47-67). It would have been obvious for a person of ordinary skill at the time of the invention to utilize the apparatus/method of (Keene, Dresser et al., Bril et al., Eglit et al.) then apply the frame memory organizing method taught by Coelho et al. to obtain the combined apparatus/method (Keene, Dresser et al., Bril et al., Eglit et al., and Coelho et al.) because it would result in reduction of buffer storage requirement and higher processing efficiency as taught by Coelho et al.(see column 1, lines 64-67). This corresponds to the claimed display controller and associated method wherein at least one byte lane comprises a plurality of pairs of byte lanes, each pair of the plurality of pairs of byte lanes for storing pairs of luminance data as well as chrominance difference data for one line of one frame of video data.

11. Claims 9, 10, 11, 20, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keene, further in view of Dresser et al., further in view of Bril et al., and further in view of Eglit et al., further in view of Coelho et al. and further in view of Selwan et al.

12. In reference to claim **9, 10, 11, 20, 21 and 22** , reference (Keene, Dresser et al., Bril et al., Eglit et al., and Coelho et al.) further discloses the fact that, those skilled in the art, know that not all the color information are required for processing because human eye is much less sensitive to color changes than it is to intensity changes; this implies that once every other line has updated chrominance data, a person of ordinary skill in the art would realize that there is no need to update chrominance data for the adjacent line: replication of chrominance data is sufficient. It also teaches interpolation and dithering techniques utilized during reconstruction of a digital video frame (see Coelho et al., column 1 , lines 29-34, 40-41, column 3, lines 9-14). However it fails to teach a bit block transfer engine for performing that aforementioned replicating function. Reference Selwan et al.(U.S.Patent 5,526,025) discloses an apparatus/method for performing run length tagging by the use of BITBLT circuit (1106), BITBLT tag generation circuit block (1202), FIFO controller (1220) sending a signal on bus (1228) to alert display memory controller (1210) to stop loading data at FIFO full condition; this corresponds to the claimed signal ouput to a host processor indicating completion of bit block transfer operation. It further discloses two standard types of BITBLT transfers(from system CPU to display memory, and from video to video(moving data blocks from one location to another) (see Seiwan et al., figures 11 and 12, column 13, lines 24-29, column 17, lines 24-26, lines 42-50, column 18, lines 59-67, and column 19, lines 1-4). It would have been obvious for a person of ordinary skill

in the art at the time of the invention to utilize the apparatus/method of (Keene, Dresser et al., Bril et al., Eglit et al., and Coelho et al.) then add a bit block transfer engine for data replication featuring an output signal(coupling to host CPU interface as referred in paragraph 7 above) alerting system CPU after FIFO is full or the end of contiguous memory block is reached, as taught by Selwan et al. to obtain the combined apparatus/method (Keene, Dresser et al., Bril et al., Eglit et al., Coelho et al.-Selwan et al.) because it would result in reduction of memory access(during critical refresh process) and power consumption, and a more responsive machine, as taught by Selwan et al.(see column 3, lines 14-16, and column 24, lines 22-27). This corresponds to the claimed display controller and associated method, wherein said chrominance difference data is stored in every other line of each of said plurality of pairs of byte lanes and said display controller further comprises a bit block transfer engine for transferring blocks of data within the display memory, wherein said bit block transfer engine replicates chrominance data from every other line of said plurality of pairs of byte lanes to a corresponding adjacent line within said plurality of pairs of byte lanes after said display memory controller has completed storing one frame of video data in the display memory, wherein said display controller outputs a signal through said bus interface to a host processor indicating completion of a bit block transfer operation.

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

14. U.S. Patent No. 5,654,773 Kajimoto et al.

The reference Kajimoto et al., is made of record as it discloses the use of a picture storage device for storing input color picture data, which is used in conjunction with an electronic still camera or a video camera.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Francis Nguyen whose telephone number is (703) 308-8858. The examiner can normally be reached on weekdays from 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe, can be reached on (703) 305-4709. The fax phone number for this Group is (703) 308-9051.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Francis Nguyen

December 8th, 1997

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
GROUP 2700